WHAT IS CLAIMED IS:

1. A semiconductor device operated in accordance with a mode selected from a plurality of modes, the semiconductor device comprising:

a plurality of mode setting fuse circuits, each generating a setting code that designates the mode and a determination signal that indicates whether the setting code is designated;

a fuse information selection circuit connected to the mode setting fuse circuits for selecting one of the setting codes in accordance with at least one of the determination signals; and

an invalidating fuse circuit for generating an invalidating signal to invalidate the selected setting code.

2. The semiconductor device according to claim 1, further comprising:

a determination circuit connected to the invalidating fuse circuit and to the mode setting fuse circuits for generating a selection signal that instructs validation or invalidation of the selected setting code in accordance with the invalidating signal.

3. The semiconductor device according to claim 2, further comprising a switching circuit connected to the determination circuit and the fuse information selection circuit, wherein the switching circuit invalidates the selected setting code when the selection signal instructs the invalidation of the setting code and validates an external setting code that is in accordance with an external mode setting signal.

4. The semiconductor device according to claim 3, wherein the mode setting signal is generated in a predetermined processing cycle by execution of a program.

5. The semiconductor device according to claim 1, wherein each of the plurality of mode setting fuse circuits includes a plurality of mode storage fuses that are broken in accordance with the setting code and a determination fuse that breaks when at least one of the mode storage fuses is broken.

6. The semiconductor device according to claim 5, wherein the number of mode storage fuses and the determination fuse is the same in each of the mode setting fuse circuits.

7. The semiconductor device according to claim 5, wherein the invalidating fuse circuit has at least one fuse, the number of all of the fuses in each mode setting fuse circuit being greater than the number of the at least one fuse in the invalidating fuse circuit.

8. The semiconductor device according to claim 1, wherein the plurality of mode setting fuse circuits include a first mode setting fuse circuit having low priority and a second mode setting fuse circuit having high priority, and wherein the fuse information selection circuit selects one of the setting codes in accordance with the determination signal of the second mode setting fuse circuit.

9. The semiconductor device according to claim 1, further comprising a memory core that is partially refreshed in a selective manner, wherein the setting code includes

refreshing information of the capacity that is to be refreshed in the memory core.

10. The semiconductor device according to claim 9, wherein the refreshing information includes an address of the section of the memory core that is to be refreshed.

11. A semiconductor device operated in accordance with a mode selected from a plurality of modes, the semiconductor device comprising:

a plurality of mode setting fuse circuits, each generating a setting code that designates the mode and a determination signal that indicates whether the setting code is designated;

a priority setting circuit connected to the mode setting fuse circuits for generating a priority signal that determines the priority order of the setting codes of the mode setting fuse circuits in accordance with the determination signals of the mode setting fuse circuits;

a fuse information selection circuit connected to the mode setting fuse circuits for selecting one of the setting codes in accordance with the priority signal; and

an invalidating fuse circuit connected to the priority setting circuit for generating an invalidating signal to invalidate the selected setting code and an altering signal that changes the priority order.

12. The semiconductor device according to claim 11, further comprising:

a determination circuit connected to the invalidating fuse circuit to generate a selection signal that instructs validation or invalidation of the selected setting code in accordance with the invalidating signal.

13. The semiconductor device according to claim 12, further comprising a switching circuit connected to the determination circuit and the fuse information selection circuit, wherein the switching circuit invalidates the selected setting code when the selection signal instructs the invalidation of the setting code and validates an external setting code that is in accordance with an external mode setting signal.

14. The semiconductor device according to claim 12, wherein the mode setting signal is generated in a predetermined processing cycle by execution of a program.

15. The semiconductor device according to claim 11, wherein each of the plurality of mode setting fuse circuits includes a plurality of mode storage fuses that are broken in accordance with the setting code and a determination fuse that breaks when at least one of the mode storage fuses is broken.

16. The semiconductor device according to claim 15, wherein the number of mode storage fuses and the determination fuse is the same in each of the mode setting fuse circuits.

17. The semiconductor device according to claim 15, wherein the invalidating fuse circuit has at least one fuse, the number of all of the fuses in each mode setting fuse circuit being greater than the number of the at least one fuse in the invalidating fuse circuit.

18. The semiconductor device according to claim 11, wherein the invalidating fuse circuit includes an

invalidating fuse and generates the invalidation signal in accordance with the breakage state of the invalidating fuse.

19. The semiconductor device according to claim 18, wherein the invalidating fuse circuit includes an altering fuse, generates the altering signal in accordance with the breakage state of the altering fuse, and provides the altering signal to the priority setting circuit.

20. The semiconductor device according to claim 11, further comprising a memory core that is partially refreshed in a selective manner, wherein the setting code includes refreshing information of the capacity that is to be refreshed in the memory core.

21. The semiconductor device according to claim 20, wherein the refreshing information includes an address of the section of the memory core that is to be refreshed.

22. A method for controlling a semiconductor device operated in a mode that is in accordance with a setting code, the method comprising:

setting a first setting code with a first mode setting fuse circuit;

setting a second setting code with a second mode setting fuse circuit; and

selecting one of the first and second setting codes.

23. The method according to claim 22, further comprising:

selecting an external setting code that is in accordance with an external mode setting signal when the first and second setting codes are not set.

24. The method according to claim 22, further comprising:

invalidating the first and second setting codes and validating an external setting code that is in accordance with an external mode setting signal using an invalidating fuse circuit.

25. A method for controlling a semiconductor device operated in a mode that is in accordance with a setting code, the method comprising:

setting a first setting code with at least one of a plurality of mode setting fuse circuits;

setting a second setting code in accordance with an external mode setting signal; and

validating one of the first and second setting codes.

26. A method for controlling a semiconductor device operated in a mode that is in accordance with a setting code, the method comprising:

setting a first setting code with a first mode setting fuse circuit;

setting a second setting code with a second mode setting fuse circuit;

selecting one of the first and second setting codes in accordance with a predetermined priority order; and

validating one of the selected setting code and an external setting code that is in accordance with an external mode setting signal.

27. The method according to claim 26, wherein said validating includes validating the external setting code when a fuse of the first mode setting fuse circuit and a fuse of the second mode setting fuse circuit are not broken.

28. The method according to claim 26, wherein said validating includes validating the first setting code when a fuse of the first mode setting fuse circuit is broken and a fuse of the second mode setting fuse circuit is not broken.

29. The method according to claim 26, wherein said validating includes validating the second setting code when a fuse of the first mode setting fuse circuit is broken and a fuse of the second mode setting fuse circuit is broken.

30. The method according to claim 26, wherein said validating includes validating the external setting code by breaking an invalidating fuse when a fuse of the first mode setting fuse circuit is broken and a fuse of the second mode setting fuse circuit is broken.

31. The method according to claim 30, wherein said validating includes validating the first setting code by breaking an altering fuse when the fuse of the first mode setting fuse circuit is broken and the fuse of the second mode setting fuse circuit is broken.

32. A method for controlling a semiconductor device including a plurality of mode setting fuse circuits and an invalidating fuse, wherein the semiconductor device enters one of a first state in which fuses of the mode setting fuse circuits are not broken, a second state in which the fuse of at least one of the mode setting fuse circuits is broken, and a third state in which the fuse of at least one of the mode setting fuse circuits is broken and the invalidating fuse is broken, the method comprising:

designating a mode of the semiconductor device in accordance with an external mode setting signal when the

semiconductor device is in the first state;

designating a mode that is in accordance with a setting code set by at least one of the mode setting fuse circuits when the semiconductor device is in the second state; and

designating the mode in accordance with the external mode setting signal when the semiconductor device is in the third state.

33. A method for controlling a semiconductor device including a first mode setting fuse circuit, a second mode setting fuse circuit, an invalidating fuse, and an altering fuse, wherein the semiconductor device enters one of a first state in which fuses of the first and second mode setting fuse circuits are not broken, a second state in which the fuse of the first mode setting fuse circuit is broken and a fuse of the second mode setting fuse circuit is not broken, a third state in which the fuse of the second mode setting fuse circuit is broken and the fuse of the first mode setting fuse circuit is not broken, a fourth state in which the fuse of at least one of the first and second mode setting fuse circuits is broken and the invalidating fuse is broken, and a fifth state in which the altering fuse is broken, the method comprising:

designating a mode of the semiconductor device in accordance with an external mode setting signal when the semiconductor device is in the first state;

designating a mode that is in accordance with a setting code set by the first mode setting fuse circuit when the semiconductor device is in the second state;

designating a mode that is in accordance with a setting code set by the second mode setting fuse circuit when the semiconductor device is in the third state; and

designating the mode that is in accordance with the

setting code set by the first mode setting fuse circuit when the semiconductor device is in the fifth state.

34. A method for controlling a semiconductor device operated in a mode that is in accordance with a setting code selected from a plurality of setting codes including setting codes stored in a plurality of mode setting fuse circuits, which includes a first mode setting fuse circuit and a second mode setting fuse circuit, and a setting code corresponding to an external mode setting signal, the method comprising:

selecting one of the following for validation:

the setting code corresponding to the external mode setting signal, which is validated by maintaining the mode setting fuse circuits in a state in which fuses of the mode setting fuse circuits are not broken;

the setting of a mode that is in accordance with the setting code of the first mode setting fuse circuit, which is validated by breaking the fuse of the first mode setting fuse circuit;

the setting of a mode that is in accordance with the setting code of the second mode setting fuse circuit, which is validated by breaking the fuse of the second mode setting fuse circuit; and

the setting of a mode that is in accordance with the external mode setting signal, which is validated by breaking the invalidating fuse; and

performing validation in accordance with the selection in the step of selecting.

35. The method according to claim 34, wherein the plurality of mode setting fuse circuits each include a determination fuse that is broken when the setting code is

set for the mode setting fuse circuit, wherein the step of selecting includes a selection for validation of:

the setting code of one of the mode setting fuse circuits in accordance with a predetermined priority order when at least two of the determination fuses are broken.

36. The method according to claim 35, wherein the semiconductor device includes an altering fuse, and the priority order is altered when the altering fuse is broken.

37. A method for controlling a semiconductor device operated in a mode that is in accordance with a setting code selected from a plurality of setting codes including setting codes stored in a plurality of mode setting fuse circuits, which includes a first mode setting fuse circuit, a second mode setting fuse circuit, and a third mode setting fuse circuit, and a setting code corresponding to an external mode setting signal, the method comprising:

selecting one of the following settings for validation:

the setting code corresponding to the external mode setting signal, which is validated by maintaining the mode setting fuse circuits in a state in which fuses of the mode setting fuse circuits are not broken;

the setting of a mode that is in accordance with the setting code of the first mode setting fuse circuit, which is validated by breaking the fuse of the first mode setting fuse circuit;

the setting of a mode that is in accordance with the setting code of the second mode setting fuse circuit, which is validated by breaking the fuse of the second mode setting fuse circuit;

the setting of a mode that is in accordance with the setting code of the third mode setting fuse

circuit, which is validated by breaking the fuse of the third mode setting fuse circuit;

the setting code of an invalidated mode setting fuse circuit in lieu of the setting code of a validated mode setting fuse circuit, which is validated by breaking an altering fuse; and

the setting of a mode that is in accordance with the external mode setting signal, which is validated by breaking the invalidating fuse and invalidating the setting of the modes that are in accordance with the first, second, and third mode setting fuse circuits; and

performing validation in accordance with the selection in the step of selecting.

38. The method according to claim 37, wherein the plurality of mode setting fuse circuits each include a mode storage fuse, which stores the setting code in accordance with the breakage state of the associated fuse, and a determination fuse, which determines whether the mode storage fuse is broken, and the step of selecting includes a selection for validation of:

determining a priority order of the setting codes of the mode setting fuse circuits that are to be validated in accordance with a breakage state of the determination fuses when the mode storage fuses of at least two of the mode setting fuse circuits are broken.

39. The method according to claim 37, wherein said selection of the setting code of an invalidated mode setting fuse circuit includes altering the priority order when the altering fuse is broken.